Refine Search

Search Results -

Terms	Documents
L9 same scan same probe	2

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L19

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, April 27, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L19	L9 same scan same probe	2	L19
L18	L1 same analizer	0	L18
L17	L9 same probe same align$	0	L17
L16	l1 and l6	0	L16
L15	l6 same probe	3	L15
L14	L1 and l5	5	L14
L13	L6 same l10	0	L13
L12	L9 same port	5	L12
L11	L10 same l9	2	L11
L10	(input or "i/O" or output) adj1 port	106459	L10
L9	L5 same on-chip	96	L9
L8	L6 same prob$	8	L8
L7	L6 and l5	7	L7
L6	(align$ adj3 signal) same captur$	93	L6

L5	logic adj1 analyzer	2027	L5
L4	L3 same data	22	L4
L3	L1 same select$	33	L3
L2	L1 same in same out	19	L2
L1	port same scan same probe	195	L1

END OF SEARCH HISTORY

L2: Entry 5 of 19 File: USPT Feb 3, 2004

DOCUMENT-IDENTIFIER: US 6687865 B1
**** See image for Certificate of Correction ****
TITLE: On-chip service processor for test and debug of integrated circuits

Detailed Description Text (26):
Another EFU of the SPU 101 is the analysis engine 215. FIG. 9a shows an embodiment of the analysis engine 215 which, under the control of the microprocessor 211, captures logic signals from the test bus 104. This is achieved by first setting either the scan flip-flops 301 of the block I/O connector circuits 310 (FIG. 4a) or the scan flip-flops 311 of the block scan connector circuit 320 (FIG. 4b) so that a boundary connection or an internal point connection of the target block 106 is selected for probing, respectively. Next, all flip-flops along the same probe string 402 are programmed (by the SPU 101) so that only signals from the selected probe point are allowed to flow through the probe string 402 and arrive at the test bus connector 401. The multiplexer 421 and the multiplexer 422 in the test bus connector 401 (FIG. 3a) are controlled by the SPU 101 so that the signals on the probe string 402 are passed along to the test bus 104. Finally, all remaining test bus connector circuits 401 along the same bit line of the test bus 104 are controlled by the SPU 101 so that they pass the probe signals along test bus 104. This allows the selected probe signal to arrive at the analysis engine 215 where it is captured for subsequent off-line analysis. The input terminals of a plurality of flip-flops 805, one for each bit line of the test bus 104, form the input port 802 of the analysis engine 215. A digital phase locked loop (PLL) 802 has selectable clock outputs 803 to each flip-flop 805 to tune when the data from each probe point is to be captured. The output terminal of each flip-flop 905 is connected to the input terminal of a variable First-In-First-Out shift register (FIFO) 804.

L4: Entry 6 of 22 File: USPT Feb 3, 2004

DOCUMENT-IDENTIFIER: US 6687865 B1
** See image for Certificate of Correction **
TITLE: On-chip service processor for test and debug of integrated circuits

Detailed Description Text (16):
A test bus connector 401 which handles a one bit connection between the test bus 104 and a test wrapper 102 is illustrated in FIG. 3b. A first multiplexer 421 has one of its input terminals connected to one of the lines of the test bus 104. The other input terminal is connected to a signal line of the test wrapper 102. The output terminal of the multiplexer 421 is connected to an input terminal of a flip-flop 426 and to an input terminal of a second multiplexer 422, which has a second input terminal connected to the output terminal of the flip-flop 426. The output terminal of the flip-flop 426 is also connected to the line of the test wrapper 102, which is also in the form of a unidirectional loop. The multiplexer 421 selects either the data from the test bus 104 or the test wrapper 102; the second multiplexer 422 selects between the data selected by the first multiplexer 431 or the data captured in the flip-flop 426 to place back onto the test bus 104. These selections are done under the control of SPU 101. The test bus connector 401 is also be used for coupling a trigger line 204, probe string line 402 or scan string line 403 to a test bus 104 by connecting the desired signal line in place of the line of the test wrapper 102 port as shown in FIG. 3b.

Detailed Description Text (26):
Another EFU of the SPU 101 is the analysis engine 215. FIG. 9a shows an embodiment of the analysis engine 215 which, under the control of the microprocessor 211, captures logic signals from the test bus 104. This is achieved by first setting either the scan flip-flops 301 of the block I/O connector circuits 310 (FIG. 4a) or the scan flip-flops 311 of the block scan connector circuit 320 (FIG. 4b) so that a boundary connection or an internal point connection of the target block 106 is selected for probing, respectively. Next, all flip-flops along the same probe string 402 are programmed (by the SPU 101) so that only signals from the selected probe point are allowed to flow through the probe string 402 and arrive at the test bus connector 401. The multiplexer 421 and the multiplexer 422 in the test bus connector 401 (FIG. 3a) are controlled by the SPU 101 so that the signals on the probe string 402 are passed along to the test bus 104. Finally, all remaining test bus connector circuits 401 along the same bit line of the test bus 104 are controlled by the SPU 101 so that they pass the probe signals along test bus 104. This allows the selected probe signal to arrive at the analysis engine 215 where it is captured for subsequent off-line analysis. The input terminals of a plurality of flip-flops 805, one for each bit line of the test bus 104, form the input port 802 of the analysis engine 215. A digital phase locked loop (PLL) 802 has selectable clock outputs 803 to each flip-flop 805 to tune when the data from each probe point is to be captured. The output terminal of each flip-flop 905 is connected to the input terminal of a variable First-In-First-Out shift register (FIFO) 804.

Detailed Description Text (36):
FIG. 12 shows a preferred embodiment of a channel of the OLA 215 which uses multiplexed PSEs 100 to combine the selection of probe points and pipelining captured data into a single, efficient design. This enables the coupling one PSE 1000 to two probe points or another PSE 1000. Scan operations shift a control

signal into the PSE 1000 to program itself to select one or the other of its input ports.

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L7: Entry 4 of 7 File: USPT Oct 21, 2003

DOCUMENT-IDENTIFIER: US 6636058 B2
TITLE: Adapter for a multi-channel, low input capacitance signal probe

Brief Summary Text (2):
The present invention relates generally to signal probe adapters and more particularly to a adapter for connecting multi-channel, low input capacitance signal probes of a measurement test instrument, such as logic analyzers and the like, to multi-channel controlled impedance connector mounted on a device under test.

Brief Summary Text (3):
Logic analyzers have long been used to acquire multiple signals from a device under test to analyze and verify timing, detect glitches, and the like. Multi-channel signal probes couple signals to the device under test from the instrument and from the device under test to the instrument. Various types of connectors are provided on the device under test, such as a microprocessor mother board, for connecting the signal probes to the device being tested. Rows of square pin connectors have traditionally been used as the interface contacts between the device under test and the probes.

Brief Summary Text (4):
The increased speed of digital circuitry requires the use of connectors having high speed, controlled impedance transmission lines. One such connector is called a mictor connector, manufactured by Tyco Electronics, Corp., Harrisburg, Pa. A mictor connector is a high speed, controlled impedance connector having a plug and closely mating receptacle. Each plug and receptacle portion is configured for either 0.025 inch or 0.050 inch center line spacing of transmission lines and contain from 38 to 266 lines. The transmission lines are aligned in parallel rows on either side of center power ground connector. The center ground connector in the plug is a corrugated planar structure that mates with vertically positioned ground leads in the receptacle. The transmission lines in the plug and receptacle are contained in mating housings. Mictor connectors have both vertically and horizontally mounted plugs and receptacles. The ends of the transmission lines extending from the bottom of the vertically mounted plug or receptacle are bent at an angle to form contact pads for soldering to contact pads on the surface of a circuit board or the like. The ends of the transmission lines of the horizontally mounted plug or receptacle extend directly outward from the bottom of the plug or receptacle for soldering to contact pads formed on opposing surfaces of the circuit board or the like at the edge of the board. The ends of the transmission lines at the other end of the housing of the plug or receptacle form electrical contacts that mate with each other when the closely mating plug and receptacle are connected together. In logic analyzer probing applications, a 38 pin mictor connector is most often used. Up to 38 circuit board runs of the device under test are laid out in pattern that terminate in a pattern corresponding to the pattern of the pins on the mictor connectors. The mictor receptacle is soldered to conductive pads that terminate the runs. In most probing applications of microprocessor boards, multiple mictor connectors are mounted on the circuit board. The multi-channel logic analyzer probe head has the mating mictor plug. The transmission lines of the mictor plug are electrically coupled to center conductors of a multiple coaxial cable type ribbon cable. Electrical elements, such as resistors, may be included in the probe head to

provide electrical isolation for the device under test.

Brief Summary Text (5):
The P6434 34-channel high density probe, manufactured and sold by Tektronix, Inc., Beaverton, Oreg., for use with the TLA family of logic analyzers is an example of a logic analyzer probe using mictor connectors. The P6434 probe head uses an edge mounted mictor connector that is soldered to contact pads on opposing sides of a circuit board. The circuit board has an additional row of interconnect contact pads formed on each opposing side of the circuit board that are electrically connected via conductive runs to the soldered contact pads of the mictor connector. The mictor connector and circuit board are inserted into a holder that also receives two probe cables. The probe cables are ribbon type cables having multiple lead wires. The lead wires of each probe cable are soldered to contact pads of a circuit board. The contact pads are electrically connected via conductive runs to another set of contact pads that match the interconnect contact pads of the mictor connector circuit board. The conductive runs preferably include resistive elements. The probe cable circuit boards are positioned on the mictor connector circuit board with electrically conductive elastomer contacts electrically connecting the contact pads on the probe cable circuit board to the interconnect contact pads of the mictor connector circuit board. The circuit boards and the mictor connector are secured in place in a housing made of opposing half shells that are screwed together.

Detailed Description Text (2):
Referring to FIG. 1, there is shown a perspective view of a measurement instrument 10, such as a logic analyzer, for injecting and acquiring signals from a device under test 12. The logic analyzer may be a portable stand alone instrument or a modular system with multiple mainframes. FIG. 1 shows one type of modular logic analyzer system 10 having a modular mainframe 14 with multiple slots for receiving various modules 16. The modules 16 include a controller module 18, one or more logic analyzer modules and pattern generator modules 20. An optional digital oscilloscope module may also be included in the system. The logic analyzer/pattern generator modules 20 are configured for a number of channels, such as 34, 68 102, 136 channels. Up to 680 channels may be included in the mainframe. Multiple mainframes may be connected together to produce a system having up to 8,120 channels. The signal outputs from the mainframe are coupled to a display device 22, such as a display monitor, for viewing the acquired signals from the device under test 12.

Detailed Description Text (14):
The present embodiment of the signal probe head 30 is designed for circuit boards having a thickness of less than 0.090 inches. In this embodiment, the flanges 134 formed adjacent to the apertures 132 in the signal contact holder 60 are removed and replaced by alignment flanges 150 extending above the circuit board 32, 36. The alignment flanges 150 extend from a retention block 152 that is positioned on the opposite side of the circuit board 32, 26 from the contact pads 40. The retention block 152 has threaded apertures 154 formed therein that are aligned with the through holes 44 in the circuit board 32, 36. The alignment flanges 150 are formed adjacent to the threaded apertures 154 and are sized to be closely receives in the through holes 44 in the circuit board 32, 36. The flanges 150 extend above the surface of the circuit board 32, 36 and include latching members 156 that extend outward from the flanges 150 and engage the top surface of the circuit board 32, 36 to secure the retention block 152 to the circuit board. The signal probe head 30 is positioned on the circuit board 32, 26 with the flanges 150 extending into the second bores 89 in the housing 50 to help align the signal probe head 50 on the board. The latching members 156 of the retention block 152 are closely received in notches 158 formed adjacent to the open end 52 of the housing 50. The attachment members 90, in the form of the threaded screws positioned in the bores 88 of the housing 50, threadably mate with the threaded apertures 154 in the retention block 152. Tightening of the threaded screws 90 in the retention block 152 captures the

circuit board 32, 36 between the retention block 152 and the signal probe head 30 and secures the signal probe head 30 to the circuit board 32, 36.

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US006636058B2

(12) **United States Patent**
Lyford

(10) **Patent No.: US 6,636,058 B2**
(45) **Date of Patent: Oct. 21, 2003**

(54) **ADAPTER FOR A MULTI-CHANNEL, LOW INPUT CAPACITANCE SIGNAL PROBE**

(75) Inventor: **J. Steve Lyford**, Portland, OR (US)

(73) Assignee: **Tektronix, Inc.**, Beaverton, OR (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/021,143**

(22) Filed: **Dec. 12, 2001**

(65) **Prior Publication Data**

US 2003/0107389 A1 Jun. 12, 2003

(51) **Int. Cl.**[7] **G01R 31/02**
(52) **U.S. Cl.** **324/754**; 439/638
(58) **Field of Search** 324/72.5, 754, 324/758, 761, 762, 158.1; 439/65, 76.1, 79, 362, 638

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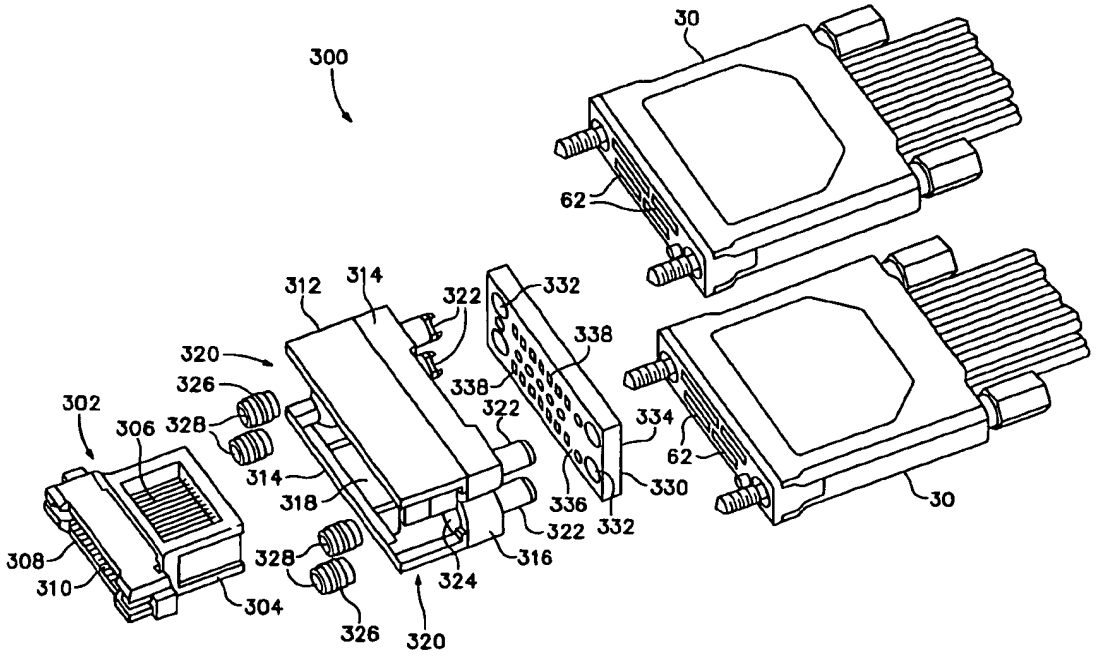
Primary Examiner—Kamand Cuneo
Assistant Examiner—Minh N. Tang
(74) *Attorney, Agent, or Firm*—William K. Bucher

(57) **ABSTRACT**

An adapter for a multi-channel, low input capacitance signal probe head has a housing with a cavity formed therein that receives one of a mating plug or receptacle portion of multi-channel, controlled impedance connector. The housing has probe head retention members formed in the sidewalls and alignment flanges disposed adjacent to the probe head retention members that are received in the signal probe head. The adapter includes a substrate having first and second arrays of contact pads formed on the respective top and bottom surfaces of the substrate. The first array of contact pads mate with electrically conductive elastomer signal contacts of the signal probe head and the second array of contact pads mate with the contact pads of the transmission lines of the plug or receptacle. Screws extend through bores in the signal probe head and engage threaded pins in the retention members.

4 Claims, 7 Drawing Sheets



L7: Entry 5 of 7 File: USPT Oct 7, 2003

DOCUMENT-IDENTIFIER: US 6631339 B2
TITLE: Data path evaluation system and method

Detailed Description Text (7):
Several alternatives are available for data collection. These may be target dependent. One method is to use the computer file containing the test signal exactly as is for the source. However, this may not be ideal since the data may get changed before it is presented to the input of DUT 10. Another method would be to capture the data at the input of DUT 10, using a logic analyzer. A logic analyzer is a device designed to capture patterns of data or voice signals. This method provides a good data source, however it may require custom setup of the logic analyzer, which is system dependent.

Detailed Description Text (17):
Turning first to the alignment stage 130, it performs the first operation in the process which is to align the signals. Since a WGN signal was used as a source, this operation may be performed by a correlation. The correlation may be performed by taking a block of the source signal and sliding it across the captured signal. The source block that is used is the first block of the source file that contains significant power. By significant power is meant power that exceeds or distinguishes from background noise. This block may be correlated against the captured signal and the result saved in an array. In addition, the energy of the source signal block may be computed as well as the energy of the overlapping part of the captured signal. Next, the array may be searched in order to find the maximum value. The index of this value may be used to adjust the captured signal such that it aligns properly with the source block. An additional check is to make sure that when the foregoing maximum value is squared, it is very close to the product of the two energies computed for the blocks of the correlation input. This ensures that a true match has been found.

CLAIMS:

1. A method comprising: transmitting a white Gaussian noise (WGN) source signal over a data path to a device under test (DUT); capturing a signal output from the DUT over the data path; aligning the captured signal with the source signal; and comparing the aligned captured signal to the source signal to determine if the signals differ.

6. The method of claim 1, wherein aligning the captured signal with the source signal comprises performing a correlation function on the captured signal.

7. The method of claim 1, wherein comparing the aligned captured signal to the source signal further comprises normalizing the aligned signals.

8. The method of claim 1, further comprising repeating aligning the captured signal with the source signal and comparing the realigned captured signal with the source signal, if the aligned captured signal differs from the source signal by a threshold.

11. An article of manufacture comprising a machine-accessible medium having content

that when accessed provides instructions to cause a machine to: transmit a white Gaussian noise (WGN) source signal over a data path to a device under test (DUT); capture a signal output from the DUT over the data path; align the captured signal with the source signal; and compare the aligned captured signal to the source signal.

16. The article of manufacture of claim 11, wherein the content to provide instructions to cause the machine to align the captured signal with the source signal comprises the content to provide instructions to cause the machine to perform a correlation function on the captured signal.

17. The article of manufacture of claim 11, wherein the content to provide instructions to cause the machine to compare the captured signal to the source signal to determine if the signals differ further comprises the content to provide instructions to normalize the aligned signals.

18. The article of manufacture of claim 11, further comprising the content to provide instructions to cause the machine to repeat aligning the captured signal with the source signal and comparing the realigned captured signal with the source signal, if the aligned captured signal differs from the source signal by a threshold.

21. A system comprising: a source host to transmit a white Gaussian noise (WGN) source signal over a data path to a device under test (DUT); a capture host to capture a signal output from the DUT over the data path; and a processor communicatively coupled with the source host and the capture host to align the captured signal with the source signal and compare the aligned captured signal to the source signal.

31. The system of claim 21, further comprising the processor to repeat aligning the captured signal with the source signal and to compare the captured signal with the source signal, if the captured signal differs from the source signal by a threshold.

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US006631339B2

(12) **United States Patent**
Poulsen et al.

(10) **Patent No.: US 6,631,339 B2**
(45) **Date of Patent: Oct. 7, 2003**

(54) **DATA PATH EVALUATION SYSTEM AND METHOD**

(75) Inventors: **Steven P. Poulsen**, East Amherst, NY (US); **Joseph S. Ott**, Depew, NY (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 185 days.

(21) Appl. No.: **09/834,016**

(22) Filed: **Apr. 12, 2001**

(65) **Prior Publication Data**

US 2002/0183952 A1 Dec. 5, 2002

(51) **Int. Cl.**[7] **G01R 27/28**; G01R 31/00

(52) **U.S. Cl.** **702/117**; 702/58; 379/15.01; 379/22.01; 375/224

(58) **Field of Search** 702/57–59, 66, 702/69–72, 112–121, 182, 189; 379/1.02, 9, 14, 18.01, 22.01, 22.02; 375/224, 226, 227; 324/523, 612, 76.11, 76.47, 76.55, 76.77; 725/107

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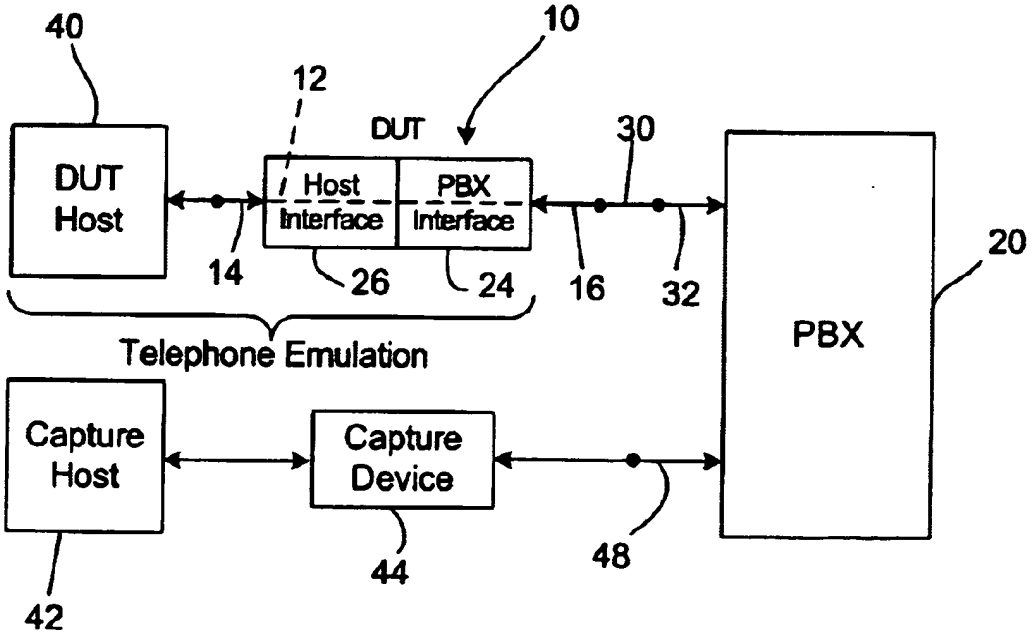
Primary Examiner—Marc S. Hoff
Assistant Examiner—Manuel L. Barbee
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman LLP

(57) **ABSTRACT**

A data path evaluation system and method is described wherein the data path can be a voice signal path and the reference signal can contain white gaussian noise.

33 Claims, 4 Drawing Sheets



US006624829B1

(12) **United States Patent**
Beck et al.

(10) **Patent No.: US 6,624,829 B1**
(45) **Date of Patent: *Sep. 23, 2003**

(54) **SYSTEM AND METHOD FOR SPECIFYING TRIGGER CONDITIONS OF A SIGNAL MEASUREMENT SYSTEM USING HIERARCHICAL STRUCTURES ON A GRAPHICAL USER INTERFACE**

(75) Inventors: **Douglas James Beck**, Colorado Springs, CO (US); **Michael A. Upham**, Colorado Springs, CO (US); **Cheryl Brown**, Colorado Springs, CO (US); **Richard A Nygaard, Jr.**, Colorado Springs, CO (US); **Natalie Overstreet Ramsey**, Colorado Springs, CO (US)

(73) Assignee: **Agilent Technologies, Inc.**, Palo Alto, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/430,197**

(22) Filed: **Oct. 29, 1999**

(51) **Int. Cl.**[7] **G06F 3/14**

(52) **U.S. Cl.** **345/771**; 345/773; 345/735; 345/739; 345/769; 702/57; 702/66; 702/67; 702/68; 702/117

(58) **Field of Search** 345/771, 773, 345/965, 835, 839, 769; 702/57, 66, 67, 68, 117

(56) **References Cited**

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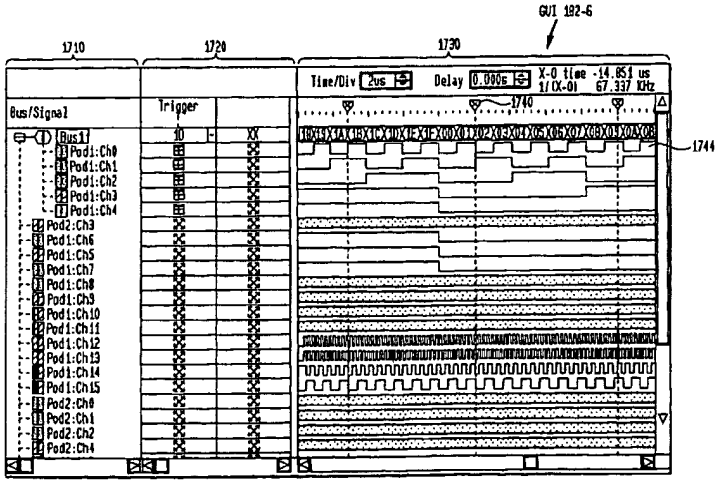
Primary Examiner—Kristine Kincaid
Assistant Examiner—Thomas T. Nguyen

(57) **ABSTRACT**

A system is disclosed for enabling a user to specify a trigger condition of a signal or bus by enabling the user to graphically select the signal or bus from a hierarchically arranged list of signal or bus names. The user may make this selection from a graphical user interface of a signal measurement system. The user also graphically selects the signal trigger condition. A trigger-specification element identifying the trigger condition is visually associated with a displayed name of the first signal or bus. The user may select the signal trigger condition of the first signal or bus by selecting the first trigger-specification element. The signal measurement system may be a logic analyzer. The hierarchically arranged list may be vertically aligned and each signal or bus name may be visually associated with one of a first group of trigger-specification elements by horizontal alignment. Each of the first group of trigger-specification elements enables the user to choose from a group of trigger condition choices consisting of any one of: rising-edge, falling-edge, either-edge, low-level, high-level, don't care, bus, positive pulse, and negative pulse. Each of the first group of trigger-specification elements may be associated with a trigger condition that occurs at a first point in time. The system further may enable a user to specify a second trigger condition of the first signal or bus by selecting from a second group of trigger-specification elements that are visually associated with the names of the plurality of signals or buses. Each of the second group of trigger-specification elements may be associated with a trigger condition that occurs at a second point in time. The second group of trigger-specification elements may be displayed to the right of the first group of trigger-specification elements. The second period of time occurs later than the first period of time.

44 Claims, 29 Drawing Sheets



L7: Entry 7 of 7 File: USPT Sep 10, 2002

DOCUMENT-IDENTIFIER: US 6447339 B1
TITLE: Adapter for a multi-channel signal probe

Brief Summary Text (2):
The present invention relates generally to signal probe adapters and more particularly to a adapter for connecting multi-channel signal probes of a measurement test instrument, such as logic analyzers and the like, to an array of signal contact pads of a device under test.

Brief Summary Text (3):
Logic analyzers have long been used to acquire multiple signals from a device under test to analyze and verify timing, detect glitches, and the like. Multi-channel signal probes couple signals to the device under test from the instrument and from the device under test to the instrument. Various types of connectors are provided on the device under test, such as a microprocessor mother board, for connecting the signal probes to the device being tested. Rows of square pin connectors have traditionally been used as the interface contacts between the device under test and the probes.

Brief Summary Text (4):
The increased speed of digital circuitry requires the use of connectors having high speed, controlled impedance transmission lines. One such connector is called a mictor connector, manufactured by Tyco Electronics, Corp., Harrisburg, Pa. A mictor connector is a high speed, controlled impedance connector having a plug and closely mating receptacle. Each plug and receptacle portion is configured for either 0.025 inch or 0.050 inch center line spacing of transmission lines and contain from 38 to 266 lines. The transmission lines are aligned in parallel rows on either side of center power ground connector. The center ground connector in the plug is a corrugated planar structure that mates with vertically positioned ground leads in the receptacle. The transmission lines in the plug and receptacle are contained in mating housings. Mictor connectors have both vertically and horizontally mounted plugs and receptacles. The ends of the transmission lines extending from the bottom of the vertically mounted plug or receptacle are bent at an angle to form contact pads for soldering to contact pads on the surface of a circuit board or the like. The ends of the transmission lines of the horizontally mounted plug or receptacle extend directly outward from the bottom of the plug or receptacle for soldering to contact pads formed on opposing surfaces of the circuit board or the like at the edge of the board. The ends of the transmission lines at the other end of the housing of the plug or receptacle form electrical contacts that mate with each other when the closely mating plug and receptacle are connected together. In logic analyzer probing applications, a 38 pin mictor connector is most often used. Up to 38 circuit board runs of the device under test are laid out in pattern that terminate in a pattern corresponding to the pattern of the pins on the mictor connectors. The mictor receptacle is soldered to conductive pads that terminate the runs. In most probing applications of microprocessor boards, multiple mictor connectors are mounted on the circuit board. The multi-channel logic analyzer probe head has the mating mictor plug. The transmission lines of the mictor plug are electrically coupled to center conductors of a multiple coaxial cable type ribbon

cable. Electrical elements, such as resistors, may be included in the probe head to provide electrical isolation for the device under test.

Brief Summary Text (5):
The P6434 34-channel high density probe, manufactured and sold by Tektronix, Inc., Beaverton, Oreg., for use with the TLA family of logic analyzers is an example of a logic analyzer probe using mictor connectors. The P6434 probe head uses an edge mounted mictor connector that is soldered to contact pads on opposing sides of a circuit board. The circuit board has an additional row of interconnect contact pads formed on each opposing side of the circuit board that are electrically connected via conductive runs to the soldered contact pads of the mictor connector. The mictor connector and circuit board are inserted into a holder that also receives two probe cables. The probe cables are ribbon type cables having multiple lead wires. The lead wires of each probe cable are soldered to contact pads of a circuit board. The contact pads are electrically connected via conductive runs to another set of contact pads that match the interconnect contact pads of the mictor connector circuit board. The conductive runs preferably include resistive elements. The probe cable circuit boards are positioned on the mictor connector circuit board with electrically conductive elastomer contacts electrically connecting the contact pads on the probe cable circuit board to the interconnect contact pads of the mictor connector circuit board. The circuit boards and the mictor connector are secured in place in a housing made of opposing half shells that are screwed together.

Detailed Description Text (2):
Referring to FIG. 1, there is shown a perspective view of a measurement instrument 10, such as a logic analyzer, for injecting and acquiring signals from a device under test 12. The logic analyzer may be a portable stand alone instrument or a modular system with multiple mainframes. FIG. 1 shows one type of modular logic analyzer system 10 having a modular mainframe 14 with multiple slots for receiving various modules 16. The modules 16 include a controller module 18, one or more logic analyzer modules and pattern generator modules 20. An optional digital oscilloscope module may also be included in the system. The logic analyzer/pattern generator modules 20 are configured for a number of channels, such as 34, 68102, 136 channels. Up to 680 channels may be included in the mainframe. Multiple mainframes may be connected together to produce a system having up to 8,120 channels. The signal outputs from the mainframe are coupled to a display device 22, such as a display monitor, for viewing the acquired signals from the device under test 12.

Detailed Description Text (14):
The present embodiment of the signal probe head 30 is designed for circuit boards having a thickness of less than 0.090 inches. In this embodiment, the flanges 134 formed adjacent to the apertures 132 in the signal contact holder 60 are removed and replaced by alignment flanges 150 extending above the circuit board 32, 36. The alignment flanges 150 extend from a retention block 152 that is positioned on the opposite side of the circuit board 32, 26 from the contact pads 40. The retention block 152 has threaded apertures 154 formed therein that are aligned with the through holes 44 in the circuit board 32, 36. The alignment flanges 150 are formed adjacent to the threaded apertures 154 and are sized to be closely receives in the through holes 44 in the circuit board 32, 36. The flanges 150 extend above the surface of the circuit board 32, 36 and include latching members 156 that extend outward from the flanges 150 and engage the top surface of the circuit board 32, 36 to secure the retention block 152 to the circuit board. The signal probe head 30 is positioned on the circuit board 32, 26 with the flanges 150 extending into the second bores 89 in the housing 50 to help align the signal probe head 50 on the board. The latching members 156 of the retention block 152 are closely received in notches 158 formed adjacent to the open end 52 of the housing 50. The attachment members 90, in the form of the threaded screws positioned in the bores 88 of the housing 50, threadably mate with the threaded apertures 154 in the retention block

152. Tightening of the threaded screws 90 in the retention block 152 captures the circuit board 32, 36 between the retention block 152 and the signal probe head 30 and secures the signal probe head 30 to the circuit board 32, 36.

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US006447339B1

(12) **United States Patent**
Reed et al.

(10) **Patent No.: US 6,447,339 B1**
(45) **Date of Patent: Sep. 10, 2002**

(54) **ADAPTER FOR A MULTI-CHANNEL SIGNAL PROBE**

(75) Inventors: **Gary W. Reed**, Beaverton; **J. Steve Lyford**, Portland, both of OR (US)

(73) Assignee: **Tektronix, Inc.**, Beaverton, OR (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/021,768**

(22) Filed: **Dec. 12, 2001**

(51) **Int. Cl.**[7] **H01R 33/90**
(52) **U.S. Cl.** **439/638**; 439/289
(58) **Field of Search** ..... 439/65, 638, 289, 439/362, 363, 323, 365, 86, 91, 76.1; 324/72.5, 758, 158 R

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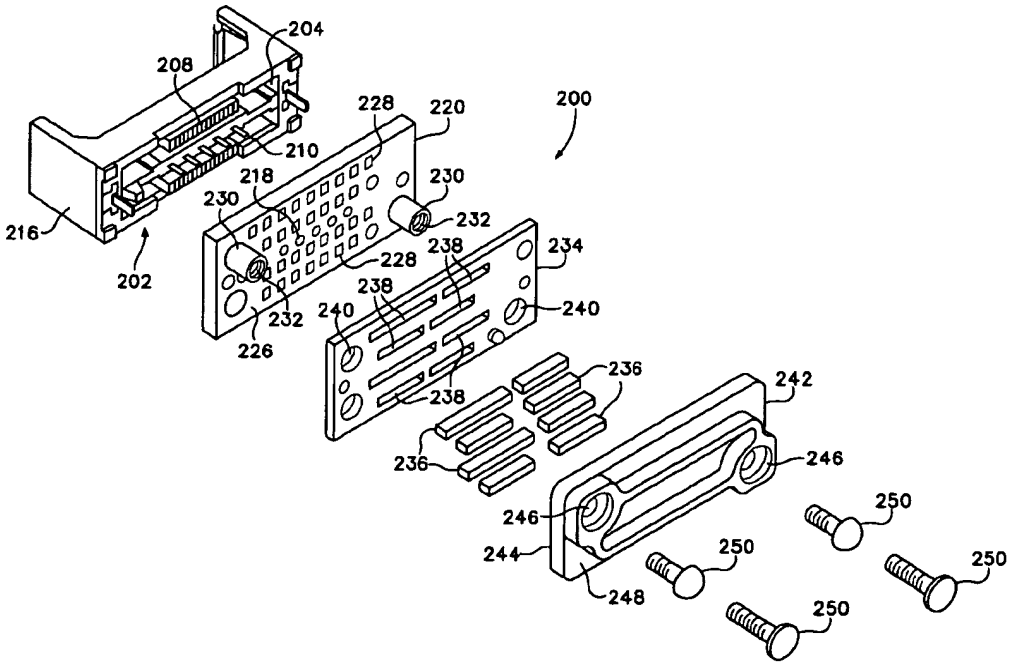
Primary Examiner—P. Austin Bradley
Assistant Examiner—Alexander Gilman
(74) *Attorney, Agent, or Firm*—William K. Bucher

(57) **ABSTRACT**

An adapter for a multi-channel signal probe has one of the mating plug or receptacle portions of the connector electrically coupled to a first array of contact pads on one surface of a substrate. A second array of contact pads corresponding to the signal contact pads on a device under test is formed on the other surface of the substrate. A removable signal contact holder supports electrically conductive elastomer signal contacts that couple the second array of contact pads to the signal contact pads of the device under test. The adapter is secured to the device under test using an adapter retention member that is positioned on the opposite of the circuit board from the signal contact pads. Screws attach the retention member to the adapter via through holes formed in the device under test.

8 Claims, 7 Drawing Sheets



L4: Entry 16 of 22 File: USPT May 14, 2002

DOCUMENT-IDENTIFIER: US 6389565 B2
TITLE: Mechanism and display for boundary-scan debugging information

Brief Summary Text (7):
To run a boundary scan test requires that the circuit under test include boundary scan functionality. FIG. 1 is a block diagram of a boundary scan component 100. Boundary scan component 100 includes internal logic 106 that is coupled to receive input data via input pins 102 and to output output data via output pins 104. Each input pin 102 and output pin 104 of interest is coupled to a separate boundary cell 110 in a boundary scan register 108. Boundary scan cells 110 are coupled serially in a loop configuration. Boundary scan test pins TDI 112, TCK 114, TDO 116, and TMS 118 are provided as dedicated boundary scan test pins that have the ability to electrically contact bed-of-nails fixture probes. Test Clock (TCK) pin 114 and Test Mode Select (TMS) pin 118 are both coupled to a Test Access Port (TAP), and are used to implement a boundary scan communication protocol. At any given time, Test Data In (TDI) pin 112 and Test Data Out (TDO) pin 116 are each switchably coupled to one of the boundary scan register 108, an instruction register 140, or a bypass register 150.

US006389565B2

(12) **United States Patent**
Ryan et al.

(10) **Patent No.: US 6,389,565 B2**
(45) **Date of Patent: *May 14, 2002**

(54) **MECHANISM AND DISPLAY FOR BOUNDARY-SCAN DEBUGGING INFORMATION**

(75) Inventors: **Heather M. Ryan; Kenneth P. Parker,** both of Fort Collins; **Robert Mayrus Tromp,** Loveland, all of CO (US)

(73) Assignee: **Agilent Technologies, Inc.,** Palo Alto, CA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/086,805**

(22) Filed: **May 29, 1998**

(51) **Int. Cl.**[7] **H02H 3/05**; H03K 19/003; H04B 1/74; H04L 1/22; H05K 10/00

(52) **U.S. Cl.** **714/724**; 345/100; 345/186; 714/727

(58) **Field of Search** 714/726, 727, 714/46, 719, 723, 25; 326/38–39; 345/431, 186, 549, 440, 434, 443, 548, 117, 100; 703/20–21; 710/22; 716/5

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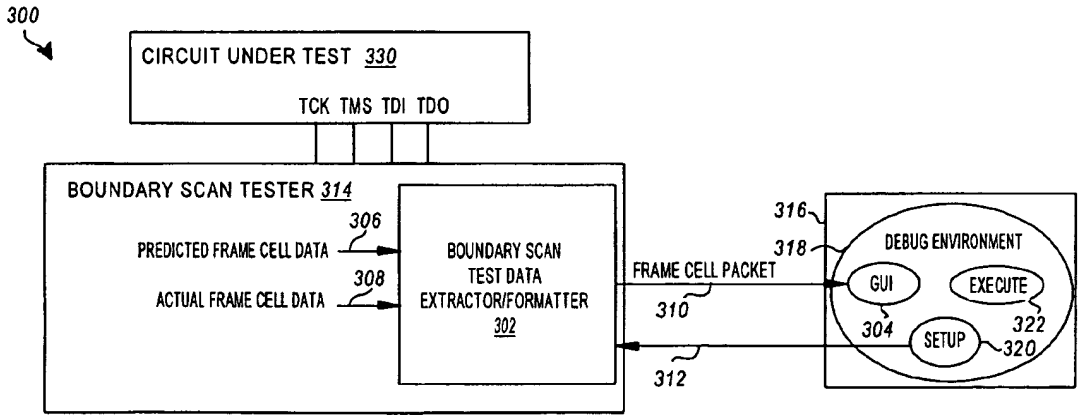
Primary Examiner—Albert Decady
Assistant Examiner—Guy Lamarre

(57) **ABSTRACT**

A graphical user interface for displaying boundary scan test data, and method for producing the same, is presented. The user interface display allows a user to view boundary scan test data from a boundary scan testing device in a format well-suited for debugging. Serial data received from the testing device is organized into a parallel format to display predicted versus actual data values on a per node basis, to show how a node is passing or failing. In a preferred embodiment, the user views the frame cell number in the boundary scan chain, the device cell number within a device at that point of the chain, the device name, the pin of the device associated with the cell, the node associated with the pin, the predicted value for the cell, the actual value for the cell as if differs from the predicted value if it differs, and the cell numbers for drivers that match predicted and actual data. Frame cells can be displayed in numerical or sorted boundary scan chain order, failing status only, or passing status only. The preferred embodiment display has the capability to display interesting correlations in the data to assist the user in debugging the circuit under test, including devices driving at fail, devices receiving at fail, devices driving only passes, devices receiving only passes, nodes always failing, nodes sometimes failing, and nodes always passing.

20 Claims, 7 Drawing Sheets



L4: Entry 20 of 22 File: USPT Dec 26, 1995

DOCUMENT-IDENTIFIER: US 5479652 A
** See image for Certificate of Correction **
** See image for Reexamination Certificate **
TITLE: Microprocessor with an external command mode for diagnosis and debugging

Abstract Text (1):
A microprocessor is disclosed herein having an external command mode for directly accessing the execution unit, responsive to externally generated commands and instructions. An external instruction path is provided, as well as a conventional processor-driven instruction path. A multiplexer is provided that selects which of the instruction paths is actually supplied to the execution unit. Using the external command mode, the user can examine and modify registers, memory, and I/O space without otherwise affecting their contents. Any instruction executable by the execution unit is executable in the external command mode. Because direct access is provided into the execution unit, there is no implicit updating that would otherwise affect the state of the processor and require saving to an alternate memory. The present invention is implemented with a conventional test access port designed in accordance with the IEEE 1149.1 boundary scan standard, with modification to include an instruction register, a data register, and control logic. The external command mode is applicable to single and multiple pipeline processors. The circuit described herein includes several selectors for selecting between the probe mode and the processor-driven mode of operation, including an external pin, an external command, and a debug exception. For ascertaining if the circuit is in the external command mode, an acknowledge pin is provided to indicate when the execution unit is ready to accept an instruction in the probe model.

Detailed Description Text (8):
In the preferred embodiment, the access port 12 has the form of a standard test access port (TAP) designed in accordance with the IEEE 1149.1 Boundary Scan standard, and uses the Joint Test Access Group (JTAG) protocol for communications. As part of the JTAG requirements, minimum features are required for such a TAP. The IEEE specification 1149.1 specifies a mechanism for adding optional features to the TAP. For the preferred embodiment the probe instruction register 36 and the probe data register 38 are implemented as "test data registers" in accordance with adding optional features in the IEEE specification 1149.1. TAP instructions are provided to access these registers 36, 38, and to perform the control illustrated by the box 40. In summary, the access port 12 has a JTAG interface, as described in IEEE standard 1149.1, which allows data and instructions to be exchanged between the access port 12 and an external signal 32. In accordance with the IEEE standard 1149.1 five pins (not shown) provide a serial interface between the external signal 32 and the processor 10. These pins include the test data in (TDI) pin and the test data out (TDO) pin. The TDI pin is used shift data or instructions into the access port 12 in a serial manner. The TDO pin shifts out the response data. The test mode select (TMS) pin is used to control the state of the access port controller. The test clock (TCK) is provided through the TCK pin. Typically, inputs are sampled on the rising edge of this signal. The test-logic-reset-state pin (TRST) pin forces the access port controller into the test logic reset state. For further information, refer to the IEEE standard 1149.1.

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L4: Entry 21 of 22 File: USPT May 23, 1995

DOCUMENT-IDENTIFIER: US 5418470 A
TITLE: Analog multi-channel probe system

Detailed Description Text (4):
A standard IEEE 1149.1 boundary scan interface 30, or similar program bus, is provided for programming the analog multi-channel probe system. A test access port (TAP) controller 32 provides appropriate signals from a test clock TCK and a test master signal TMS. Test input data TDI is loaded serially into a control register 34, an instruction register 36 and a bypass register 38. A test data output multiplexer 40 is coupled to have as inputs the outputs from the control register 34, the instruction register 36 and the bypass register 38 to provide test output data TDO back to the boundary scan interface. A decoder logic circuit 42 converts the contents of the control register 34 into respective enable/select signals for the input and output buffer amplifiers 12, 16, the routers and routing switches 14, 24, and the termination circuits 28.

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L4: Entry 18 of 22 File: USPT Dec 5, 2000

DOCUMENT-IDENTIFIER: US 6158034 A
TITLE: Boundary scan method for terminating or modifying integrated circuit operating modes

Brief Summary Text (4):
IEEE/ANSI standard 1149.1 - 1990, also known as JTAG and Boundary Scan, is a standard for testing integrated circuits as well as circuit boards. In the prior art, printed circuit boards were tested by automatic test equipment (ATE) which contacted special locations on a board by means of probe wires attached to a probe card. The probe card interfaced with the ATE in a manner such that test signals could be sent to and from the ATE to specific areas of a board under test. On the other hand, Boundary Scan requires that certain registers and dedicated pins be placed on a chip so that software can be used to implement test procedures, rather than ATE. Relatively inexpensive computers can now be used to test integrated circuit chips even after the chip is manufactured and shipped. Five dedicated pins provided on chips with a Boundary Scan test capability communicate with a Test Access Port (TAP) which gives access to logic which executes Boundary Scan and other test procedures. The pins are Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), Test Mode Select (TMS) and Test Reset (TRST).

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US006266744B1

(12) **United States Patent**
Hughes et al.

(10) **Patent No.: US 6,266,744 B1**
(45) **Date of Patent: Jul. 24, 2001**

(54) **STORE TO LOAD FORWARDING USING A DEPENDENCY LINK FILE**

(75) Inventors: **William Alexander Hughes**, Burlingame, CA (US); **Derrick R. Meyer**, Austin, TX (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/313,873**

(22) Filed: **May 18, 1999**

(51) **Int. Cl.**[7] **G06F 12/00**; G06F 15/00

(52) **U.S. Cl.** **711/146**; 711/126; 711/123; 711/156; 712/23; 712/216; 712/217

(58) **Field of Search** 711/126, 146, 711/123, 156, 23; 712/216, 217

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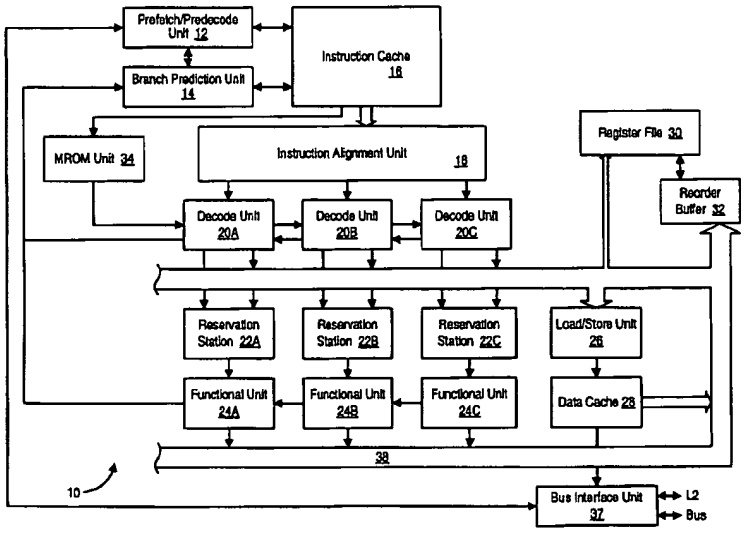
Primary Examiner—Matthew Kim
Assistant Examiner—B. R. Peugh
(74) *Attorney, Agent, or Firm*—Conley, Rose & Tayon, PC; Lawrence J. Merkel

(57) **ABSTRACT**

A processor employing a dependency link file. Upon detection of a load which hits a store for which store data is not available, the processor allocates an entry within the dependency link file for the load. The entry stores a load identifier identifying the load and a store data identifier identifying a source of the store data. The dependency link file monitors results generated by execution units within the processor to detect the store data being provided. The dependency link file then causes the store data to be forwarded as the load data in response to detecting that the store data is provided. The latency from store data being provided to the load data being forwarded may thereby be minimized. Particularly, the load data may be forwarded without requiring that the load memory operation be scheduled.

24 Claims, 17 Drawing Sheets



United States Patent [19]

Jacobs et al.

[11] **Patent Number: 4,817,093**

[45] **Date of Patent: Mar. 28, 1989**

[54] **METHOD OF PARTITIONING, TESTING AND DIAGNOSING A VLSI MULTICHIP PACKAGE AND ASSOCIATED STRUCTURE**

[75] Inventors: **Scott L. Jacobs**, Apex, N.C.; **Maurice T. McMahon, Jr.**, Poughkeepsie; **Perwaiz Nihal**, Hopewell Junction, both of N.Y.; **Burhan Ozmat**, Dallas, Tex.; **Henri D. Schnurmann**, Monsey; **Arthur R. Zingher**, White Plains, both of N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **64,976**

[22] Filed: **Jun. 18, 1987**

[51] **Int. Cl.**[4] **G06F 11/00**

[52] **U.S. Cl.** **371/25**

[58] **Field of Search** ..... 371/25, 20, 15, 27; 324/73 R, 73 AT; 364/200 MS File, 900 MS File

[56] **References Cited**

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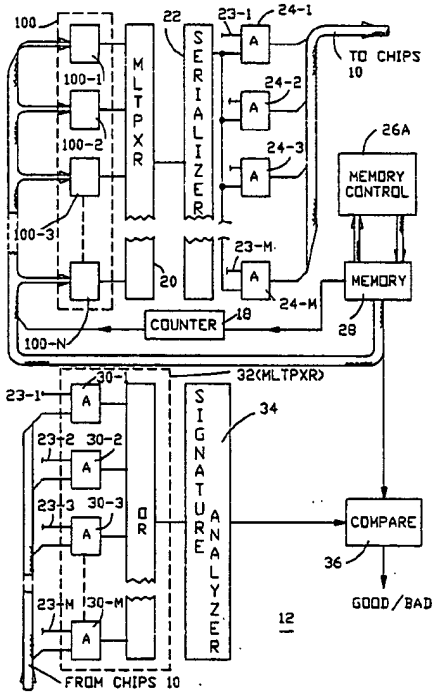
Primary Examiner—Jerry Smith
Assistant Examiner—Robert W. Beausoliel
Attorney, Agent, or Firm—Steven J. Meyers; Yen S. Yee

[57] **ABSTRACT**

A self-contained method and structure for partitioning, testing and diagnosing a multi-chip packaging structure. The method comprises the steps of electronically inhibiting all chips in the multi-chip package except for the chip or chips under test, creating a signature of the chip or chips under test by generating and applying random patterns to the chip or chips under test (referred to as the unit under test) and comparing the signature obtained to a "good machine" simulation signature. The structure comprises means for accomplishing the above method steps. A preferred structure comprises an semiconductor substrate having redundant self test circuitry built in and chips having ECIPT circuitry mounted on the semiconductor substrate. Either all or a portion of the self test circuitry, including the required multiplexers, etc., may be incorporated into the semiconductor substrate. ECIPT circuitry may also be built into the substrate below each chip site. The combination of partitioning along chip boundaries, simple and inexpensive testing without external testers or mainframe computers, and enhanced diagnostics are made possible by the present invention.

28 Claims, 6 Drawing Sheets



US005418470A

United States Patent [19]

Dagostino et al.

[11] Patent Number: 5,418,470

[45] Date of Patent: May 23, 1995

[54] **ANALOG MULTI-CHANNEL PROBE SYSTEM**

[75] Inventors: **Thomas P. Dagostino**, Beaverton; **Arnold M. Frisch**, Portland, both of Oreg.

[73] Assignee: **Tektronix, Inc.**, Wilsonville, Oreg.

[21] Appl. No.: **139,651**

[22] Filed: **Oct. 22, 1993**

[51] **Int. Cl.**[6] **G01R 31/28**

[52] **U.S. Cl.** **324/763**; 324/158.1; 371/22.5

[58] **Field of Search** ..... 324/158 F, 158 R, 73.1, 324/763, 158.1; 371/22.3, 22.5, 22.6

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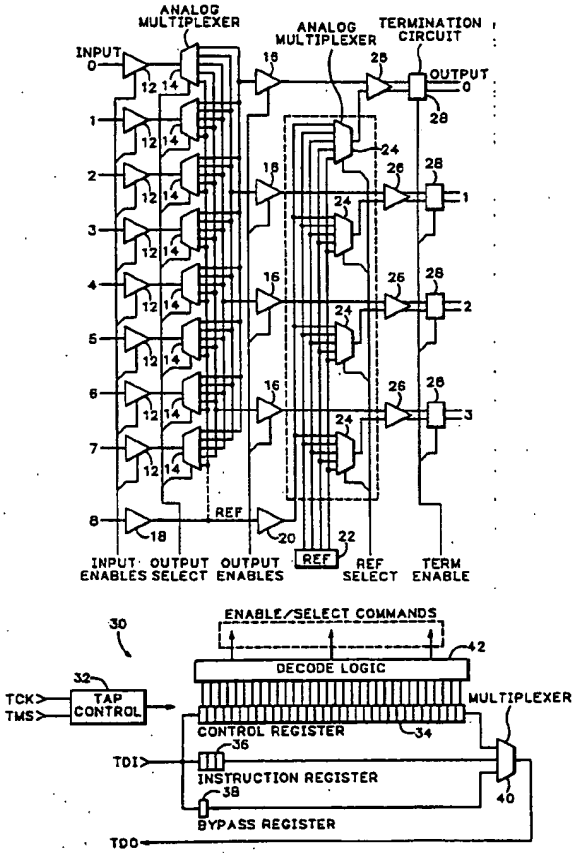
Primary Examiner—Ernest F. Karlsen
Attorney, Agent, or Firm—Francis I. Gray; John Smith-Hill

[57] **ABSTRACT**

A programmable analog multi-channel probe system is embedded within a device under test for coupling test points to external measurement points of the device under test. Programmable input buffer amplifiers are coupled to the test points to couple the data at those points to their outputs when enabled. The data from the input buffer amplifiers are input to respective routers to provide a plurality of outputs. Each common output from the routers is coupled as an input to an output buffer amplifier that provides the data as an output when enabled. The data at the output of the output buffer amplifiers is converted to a differential signal for transmission to the external measurement point by differential input/output amplifiers that have a reference level, selected from a plurality of reference levels including an internal reference level, as an input for comparison with the data from the output buffer amplifiers. A termination circuit may be provided for each output to provide appropriate impedance interface with the measurement points.

14 Claims, 2 Drawing Sheets



US005479652A

United States Patent [19]

Dreyer et al.

[11] Patent Number: 5,479,652

[45] Date of Patent: Dec. 26, 1995

[54] **MICROPROCESSOR WITH AN EXTERNAL COMMAND MODE FOR DIAGNOSIS AND DEBUGGING**

[75] Inventors: **Robert S. Dreyer**, Sunnyvale; **Donald B. Alpert**, Santa Clara; **Nimish H. Modi**, San Jose, all of Calif.; **Mike J. Tripp**, Forest Grove, Oreg.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[21] Appl. No.: **327,229**

[22] Filed: **Oct. 21, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 874,642, Apr. 27, 1992, abandoned.

[51] **Int. Cl.**[6] **G06F 11/34**

[52] **U.S. Cl.** **395/183.06**; 364/265.6; 364/267.91; 364/DIG. 1; 395/375; 395/183.08; 395/800

[58] **Field of Search** 371/15.1, 16.1, 371/19, 22.1; 364/265.6, 267.91; 395/575

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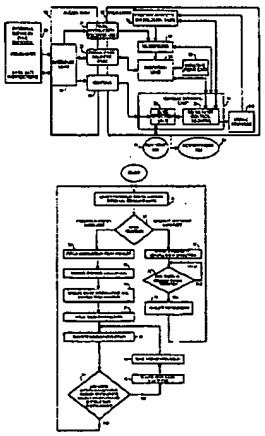
Primary Examiner—Robert W. Beausoliel, Jr.
Assistant Examiner—Albert Decady
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

A microprocessor is disclosed herein having an external command mode for directly accessing the execution unit, responsive to externally generated commands and instructions. An external instruction path is provided, as well as a conventional processor-driven instruction path. A multiplexer is provided that selects which of the instruction paths is actually supplied to the execution unit. Using the external command mode, the user can examine and modify registers, memory, and I/O space without otherwise affecting their contents. Any instruction executable by the execution unit is executable in the external command mode. Because direct access is provided into the execution unit, there is no implicit updating that would otherwise affect the state of the processor and require saving to an alternate memory. The present invention is implemented with a conventional test access port designed in accordance with the IEEE 1149.1 boundary scan standard, with modification to include an instruction register, a data register, and control logic. The external command mode is applicable to single and multiple pipeline processors. The circuit described herein includes several selectors for selecting between the probe mode and the processor-driven mode of operation, including an external pin, an external command, and a debug exception. For ascertaining if the circuit is in the external command mode, an acknowledge pin is provided to indicate when the execution unit is ready to accept an instruction in the probe model.

36 Claims, 5 Drawing Sheets



US005590354A

United States Patent [19]

Klapproth et al.

[11] Patent Number: 5,590,354

[45] Date of Patent: Dec. 31, 1996

[54] **MICROCONTROLLER PROVIDED WITH HARDWARE FOR SUPPORTING DEBUGGING AS BASED ON BOUNDARY SCAN STANDARD-TYPE EXTENSIONS**

[75] Inventors: **Peter Klapproth; Frederik Zandveld; Jacobus M. Bakker; Gerardus C. Van Loo**, all of Eindhoven, Netherlands

[73] Assignee: **U.S. Philips Corporation**, New York, N.Y.

[21] Appl. No.: **281,964**

[22] Filed: **Jul. 28, 1994**

[30] **Foreign Application Priority Data**

Jul. 28, 1993 [EP] European Pat. Off. 93202228

[51] **Int. Cl.**[6] **G06F 11/00**

[52] **U.S. Cl.** **395/800**; 395/183.06; 371/22.3; 364/232.8; 364/267.91; 364/DIG. 1

[58] **Field of Search** 395/800, 500, 395/250, 182.08, 182.19, 183.01, 183.04, 183.06, 183.11, 183.13; 371/3, 21.3, 21.6, 22.3, 23, 29.1

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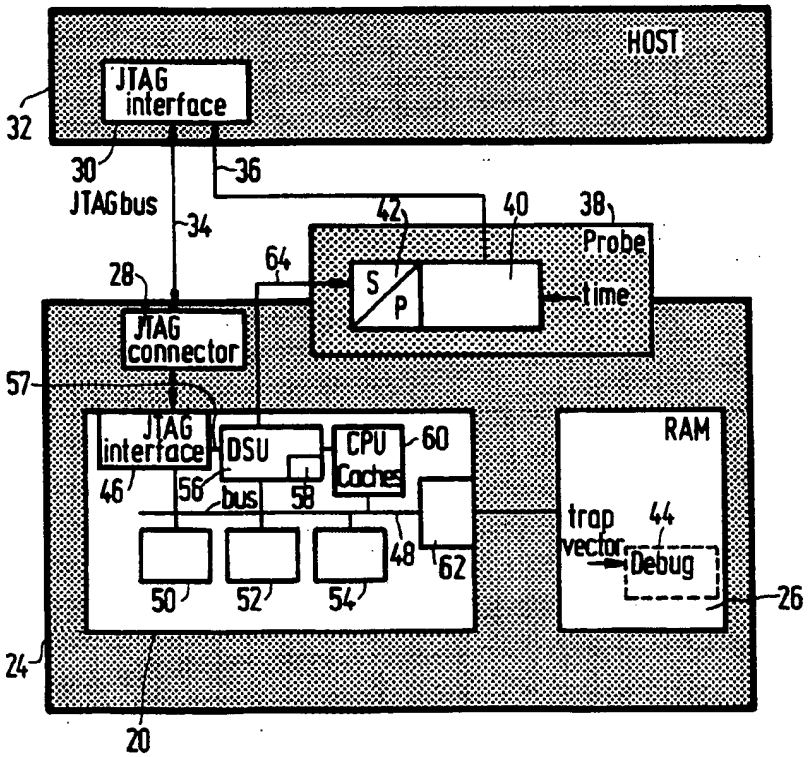
Primary Examiner—Alpesh M. Shah
Attorney, Agent, or Firm—Laurie E. Gathman

[57] **ABSTRACT**

A microprocessor includes a processor element, a memory interface element, an IO interface element, a debug support element and an internal bus interconnecting all above elements. For easy debugging, it also includes attached to the internal bus a registered boundary scan standard (JTAG) interface that accesses one or more scan chains inside the microprocessor, and is arranged for controlling DMA-type exchanges via the internal bus with other elements connected to this bus.

10 Claims, 3 Drawing Sheets



US005724505A

United States Patent [19]

Argade et al.

[11] Patent Number: 5,724,505

[45] Date of Patent: Mar. 3, 1998

[54] **APPARATUS AND METHOD FOR REAL-TIME PROGRAM MONITORING VIA A SERIAL INTERFACE**

[75] Inventors: **Pramod Vasant Argade; Michael Richard Betker**, both of Allentown; **Shaun Patrick Whalen**, Wescosville, all of Pa.

[73] Assignee: **Lucent Technologies Inc.**, Murray Hill, N.J.

[21] Appl. No.: **647,852**

[22] Filed: **May 15, 1996**

[51] **Int. Cl.**[6] **G01R 31/28**

[52] **U.S. Cl.** **395/183.21**

[58] **Field of Search** 371/22.1; 395/183.21, 395/183.1, 183.11, 183.14, 183.15, 184.01; 364/265.3, 265.6, 267, 267.2, 267.4, 267.7, 267.91, 267.8

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Primary Examiner—Hoa I. Nguyen

[57] **ABSTRACT**

A digital microprocessor having a processor core is provided with trace recording hardware capable of receiving, analyzing and temporarily storing data indicative of program instructions (i.e., instruction types) executed by the processor core and of their respective addresses. The trace recording hardware outputs an abbreviated real-time program trace, containing minimum data necessary to reconstruct a full program trace, via a JTAG port to an external debug host computer where a user may reconstruct the full program trace with reference to a program listing. The abbreviation scheme used by the trace recording hardware is preferably achieved by comparing instruction types received from the processor core to at least one pre-defined instruction type, and abbreviating or discarding the corresponding address information as a function of the particular instruction type. The trace recording hardware may be set into one of two modes by the user. In the first mode, the trace recording hardware stalls the processor core when it reaches its maximum storage capacity for instruction type and/or address data until storage becomes available. In the second mode, when the trace recording hardware becomes full it discards data received from the processor core and stores an overflow indicator. The program trace may be initiated and stopped by the user or by signals internal to the digital microprocessor.

28 Claims, 7 Drawing Sheets